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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Christopher C Winslade
McAndrews Held & Malloy
500 W Madison Street
suite 3400
Chicago, IL 60661

EXAMINER	
MEW, KEVIN D	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/028,871	BEHRENS ET AL.	
	Examiner	Art Unit	
	Kevin Mew	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final Action

Response to Amendment

1. Applicant's Remarks/Arguments filed on 11/2/2006 have been considered. Claims 8-21 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 8-9, 11-13, 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Patel (USP 4,945,538).

Regarding claim 8, Patel discloses an integrated circuit synchronous read channel (**a signal processing channel including a read signal**, col. 2, lines 63-68 and coded read signal in line 10, Fig. 1) for receiving digitized read signals representing digitized samples (**the read signal corresponds to a recorded data sequence such as the RLL code**, col. 2, lines 9-13 and 63-68) of a read signal (**a read signal**) of a magnetic storage device (**magnetic read head in a digital storage device**, col. 2, lines 63-68) and recovering digital data represented (**decoding to provide a coded binary data output**, col. 3, lines 50-54) thereby comprising:

a digital peak detector (**peak-detection channel**, col. 2, lines 65-68) for detecting characteristics of the digitized read signals indicative of storage media transitions (**for detecting the crowding of the write transitions on the media**, col. 2, lines 65-68);

a timing recovery circuitry (**a phase-locked loop timing recovery circuit**, col. 3, lines 1-9 and element 13, Fig. 1) responsive to the digitized read signals (**responsive to the read signal that corresponds to the recorded data sequence**) and the output of the digital peak detector (**using a conventional peak-detection circuit**) to provide a timing control signal (**deriving a read clock signal**, col. 3, lines 65-68) for controlling the timing of digitized samples of the read signal (**for controlling the timing of the digitized sample values at successive clock times**, col. 3, lines 65-68, col. 4, lines 1-3);

a sequence detector (**a sequence detection algorithm**, col. 2, lines 20-21) responsive to the digitized read signals for receiving a stream of the digitized read signals (**responsive and receiving digitized sample values**, col. 2, lines 9-27) and determining a corresponding sequence of binary digital signals likely to be represented thereby (**determines coded binary data from the digitized sample values**, col. 2, lines 9-27); and

an RLL(d,k) decoder (**RLL decoder**, element 23, Fig. 1) for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector (**RLL decoder to apply a decoding algorithm to the equalized digitized sample values to provide a coded binary data output in line 26**, col. 3, lines 50-52 and Fig. 1).

Regarding claim 9, Patel discloses all the aspects of the claimed invention set forth in the rejection of claim 8 above.

Patel further discloses the integrated circuit synchronous read channel of claim 8 further comprising digital pulse shaping filter circuitry (**low pass filter**, element 12, Fig. 1) for modification of the digitized read signals (**for filtering the read signals that corresponds to recorded binary RLL data sequence**, col. 3, lines 1-9, 18-21) prior to receipt thereof by at least one of (i) the sequence detector, (ii) digital peak detector and (iii) the timing recovery circuitry (**prior to receipt by the phase-locked loop timing recovery circuit**, element 13, Fig. 1).

Regarding claim 11, Patel discloses the integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes variable filter parameters (**low pass filter 12 includes variable filter parameters to compensate for the anomalies in the signal shape**, col. 6, lines 33-42).

Regarding claim 12, Patel also discloses the integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes programmable filter parameters (**low pass filter 12 includes filter parameters so that a response to a single magnetic transition is a pulse given by certain sample values**, col. 3, lines 18-25).

Regarding claim 13, Patel also discloses the integrated circuit synchronous read channel of claim 9 further comprising spectrum smoothing filter circuitry (**equalizer**, element 22, Fig. 1) for filtering the digitized read signals prior to processing by the sequence detector (**for filtering the digital sample values prior to processing by the decoder**, col. 3, lines 45-54).

In claim 15, Patel discloses the integrated circuit synchronous read channel of claim 8, wherein the sequence detector allows selection between center and side sampling of the digitized read signals (**side samples at 2 and center sample at 4**, Fig. 2B).

Regarding claim 16, Patel discloses the integrated circuit synchronous read channel of claim 8, wherein the sequence detector accommodates pulse asymmetry in the digitized read signals (**the decoder compensates for the anomalies in the signal shape**, col. 2, lines 20-27).

Regarding claim 17, Patel discloses the integrated circuit synchronous read channel of claim 8, wherein the sequence detector is a partial response sequence detector (**the channel is a partial response channel**, col.. 3, lines 10-17).

Regarding claim 18, Patel also discloses the integrated circuit synchronous read channel of claim 8, wherein the timing recovery circuit operates in at least one of an acquisition mode and a tracking mode (**phase-locked loop timing recovery circuit including a variable frequency circuit VFO which is driven by peak detection of the read signal**, col. 3, lines 65-68).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel in view of Huber (USP 5,107,379).

Regarding claim 19, Patel discloses all the aspects of the claimed invention set forth in the rejection of claim 8 above, except fails to explicitly show the integrated circuit synchronous read channel of claim 8, wherein the timing recovery circuit is programmable.

However, Huber discloses that the frequency dividers 89 and 91 (Fig. 3) of the phase locked loop are changeable according to the RLL code being used (col. 8, lines 49-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the read channel method and apparatus of Patel with the teaching of Huber in varying the frequency divider value of the phase-locked loop in accordance with the RLL code being used such that the timing recovery circuit of Patel is programmable.

The motivation to do so is to produce a data clock output such that it is consistent with the particular RLL modulated code being used.

Regarding claim 20, Patel discloses all the aspects of the claimed invention set forth in the rejection of claim 8 above, except fails to explicitly show the integrated circuit synchronous

read channel of claim 8, wherein the timing recovery circuit comprises at least one of phase error and frequency error.

However, Huber discloses a phase locked loop in a read channel detector apparatus, which produces a phase error signal between the read clock and the asynchronous data (col. 8, lines 25-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the read channel method and apparatus of Patel with the teaching of Huber in producing a signal corresponding to the phase and frequency difference between the read clock and the asynchronous data such that the timing recovery circuit of Patel comprises at least one of phase error and frequency error.

The motivation to do so is to compensate the phase error so that loop stability is reached.

4. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel in view of White (USP 4,724,496).

Regarding claim 21, Patel discloses all the aspects of the claimed invention set forth in the rejection of claim 8 above, except fails to explicitly show the integrated circuit synchronous mad channel of claim 8, wherein the timing recovery circuit computes timing error at transition times.

However, White discloses the transition time displacement errors in a peak detector that may occur directly on data and indirectly on clock signals must be taken into consideration in a phase-locked loop detection circuit (col. 3, lines 10-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the read channel method and apparatus of Patel with the teaching of White in having a phase-locked loop detection circuit to detect the transition timing errors such that the timing recovery circuit of Patel computes timing error at transition times.

The motivation to do so is to accommodate this timing error in order to avoid the slow recovery of synchronize clock signals because large timing errors of the reference data signal with respect to the VCO clock signal require averaging the timing errors from the phase comparator.

Response to Arguments

5. Applicant's arguments filed on 11/2/2006 have been fully considered but are not persuasive.

With respect to claims 8, 10, 14, applicant argued on page 1, last paragraph of the Remarks that Patel fails to disclose timing recovery circuit responsive to both digitized read signals and output of a digital peak detector, the examiner respectfully disagrees. First, the phase-locked loop clock 13 comprises a phase-locked loop timing recovery circuit (col. 3, lines 4-7), which reads on the "timing recovery circuit" cited in claims 8, 10, 14. In addition, it is claimed in line 2 of claims 8, 10, 14 that "digitized read signals representing digitized samples of a read signal" which the examiner equates as "binary data sequence coded with the (1,7) RLL code of an analog signal." Therefore, the "digitized read signals" equate to the "binary data sequence coded with the (1,7) RLL code" (col. 2, lines 67-68, col. 3, line 1). As a result, the phase-locked loop clock comprising the phase-locked loop timing recovery circuit is responsive

to the digitized read signals (binary data sequence coded with the (1,7) RLL code) and is responsive to the output of a digital peak detector because the VFO of the phase-locked loop clock comprising phase-locked loop timing recovery circuit is driven by the peak-detection circuit (col. 3, lines 65-38).

With respect to claims 8, 10, 14, applicant argued on page 2, second paragraph of the Remarks that Patel fails to disclose an RLL (d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector because the run length limited decoder of Patel is a fixed decoder while the run length limited decoder of the claimed invention is variable, the examiner respectfully disagrees. It is noted that the features upon which applicant relies (i.e., "variable run length limited decoder") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

With respect to claim 11, applicant further argued on page 3, second paragraph of the Remarks that Patel fails to disclose variable filter parameters, the examiner respectfully disagrees. It is noted that whether Patel can compensate for the anomalies or variable filter parameters is immaterial because the claimed feature recites "a digital pulse shaping filter circuitry includes variable filter parameters." Patel discloses a digital pulse shape filter that is varied based on parameters such as different radius on the surface of a magnetic disk or head geometry (col. 6, lines 33-39), which reads on the "a digital pulse shaping filter circuitry including variable filter parameters" recited in claim 11.

With respect to claim 15, applicant argued on page 3, second paragraph of the Remarks that Patel fails to disclose selection between center and side sampling of the digitized read signals at the sequence detector, the examiner respectfully disagrees. Patel discloses in Fig. 2B that there are center sampling performed at points 4 and –4 and side sampling at points 2 and –2, which reads on the claimed limitations. Further disclosure of the sample values is found in col. 3, lines 18-25 of Patel.

With respect to claims 19-20, applicant also argued on page 4, first paragraph of the Remarks that Huber '379 fails to disclose the time recovery circuit is programmable, the examiner respectfully disagrees. It is first noted that Patel discloses a phase-locked loop time recovery circuit will variable frequency oscillator VFO. Huber '379 discloses a phase-locked loop with a VFO coupled to a frequency divider and the frequency divider values are so chosen that they are consistent with the RLL modulation code used (col. 7, lines 45-48, col. 8, lines 49-61). This reads on the "time recovery circuit is programmable" because the frequency divider values are selected/programmed such that they are consistent with the RLL modulation code used.

Lastly, with respect to claim 21, applicant argued on page 4, last paragraph of the Remarks that the White reference fails to disclose "a timing recovery circuit that computes timing error at transition times," the examiner respectfully disagrees. Applicant's attention is directed to the entire passage of col. 3, lines 10-21 of White cited by the examiner, not just the first sentence. It is noted that Patel already discloses a timing receiving circuit in a phase-locked

loop except fails to disclose computing timing error at transition times. However, White discloses timing error (col. 3, lines 10-21) is determined at transition times wherein the greater the degree of transition timing error, the longer the recovery time of clock or strobe signals following transients. Therefore, White's disclosure reads on the claimed limitations of "a timing recovery circuit that computes timing error at transition times."

In light of the foregoing, claims 8-18 stand rejected under 35 U.S.C. 102(b) as being anticipated by Patel (USP 4,945,538) and claims 19-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Patel in view of Huber (USP 5,107,379).

Allowable Subject Matter

6. Claims 10, 14 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

In claim 10, an integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

delay means for delaying the coupling of the digitized read signals to the digital peak detector or the timing recovery circuit to match the delay of the coupling of the digitized read signals to the timing recovery circuitry or the digital peak detector, respectively, imposed by the digital pulse shaping filter.

In claim 14, an integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

wherein the sequence detector processes two digitized read signals at a time, the two digitized read signals representing digitized samples of a read signal of a magnetic storage device during two successive channel bit times.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-3141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Seema S. Rao 1/22/07
SEEMA S. RAO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Kevin Mew KM
Work Group 2616